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CORPORATE CHEMICAL RESEARCH LABORATORIES

P. R. MALLORY & CO. INC.

Indianapolis, Indiana

P. R. MALLORY & CO., INC.

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CELL EQUALIZATION TECHNIQUES

Contract No. AF 33(657)-8749
Task 817304-18, Project 8173

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Prepared by: W. D. Loftus

FOREWORD

This report was prepared by P. R. Mallory & Co. Inc., Indianapolis, Indiana for Aeronautical Systems Division of Wright-Patterson Air Force Base, Ohio, on Contract Number AF 33(657)-8749, Task 817304-18. It is our pleasure to acknowledge the assistance of Mr. W. S. Bishop of the Aeronautical Systems Division, who is the project engineer.

The work covered by this report was accomplished under Air Force Contract No. AF 33(657)-8749, but is being published and distributed prior to Air Force review. The publication of this report, therefore, does not constitute approval by the Air Force of the findings or conclusions contained herein. It is published for the exchange of stimulation of ideas.

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ABSTRACT

Contact resistance to silicon p-n junction structures has been reduced significantly by adjustment of process procedures and the addition of a gold plating step. Optimum nickel sintering temperature has been determined to be 500°C; lowest values of device resistance have been obtained by overplating the nickel with gold.

Work has been done on lower resistivity starting material. Characteristic slopes of 5 x 1000 amp per volt per sq in ~~5 x 10² amp/volt/in²~~ have been obtained from 0.005 ohm-cm silicon. Specific voltage as a function of resistivity has not been demonstrated in the case of germanium.

Cell equalizers and anti-reversal devices have been designed to operate with the 3.2 ampere hour nickel cadmium system. Three experimental battery charging circuits using these devices have been fabricated and operated. One sample test set has been delivered to Aeronautical Systems Division for evaluation.

I. INTRODUCTION

Space applications require reliable energy conversion and storage systems capable of unattended operation, usually over long periods of time. At the present state of technology, the space vehicle power supply system requirements are most nearly fulfilled by solar cells coupled to electrochemical batteries. In earth-orbiting satellite applications, the solar cells deliver electrical power to the batteries during the light and the batteries in turn deliver power to the load during the dark portion of a cycle. Series connection of several alkaline cells is required to provide higher than single cell operating voltages. In the interest of low weight and small size, deep cycling or the removal and restoration of an appreciable part of the battery capacity during a given cycle is desirable.

Unfortunately, certain limitations which become increasingly severe with increasing cycle depth exist in the system. Solar cell output approaches constant current over a relatively wide voltage range and this is an appropriate alkaline cell charge condition. At the present state of the rechargeable battery art, however, it is virtually impossible to produce cells of identically equal capacities and internal resistances and testing has shown the individual capacities gradually become more diverse during life of the cycled battery.[1] Due to these inherent differences, instantaneous cell terminal voltages of a battery under constant current charge are generally unequal, inferior cells reaching maximum terminal voltage before cells of higher capacity. Overcharging can results in electrolyte decomposition and cell destruction. Also, any cell in the series string not capable of discharging at the rate set by the load will be subject to forced voltage reversal and charged in the reverse direction, a condition also conducive to electrode impairment and electrolyte decomposition with gas formation which may cause catastrophic destruction of sealed cells.

The P. R. Mallory Co. submitted Aeronautical Systems Division a proposal entitled "Cell Equalization and Anti-Cell Reversal Techniques for Secondary Batteries" in response to Purchase Request No. 127425 and as a result was awarded Contract AF 33(657)-8749 effective 1 October 1962 and terminating 30 September 1963. One objective of this program is to investigate methods of equalizing the terminal voltage of individual secondary cells in a series connected group. Another objective is to investigate methods of preventing cell reversal upon discharge. The work program will include, but will not be limited to theoretical and experimental determination of a reliable method of cell equalization on charge and elimination of cell reversal on discharge. It will also embrace applied research on the equalizer and anti-reversal semiconductor devices with sufficient evaluations to determine that the method is reliable and practical. Two experimental sets including batteries shall be delivered.

II. FACTUAL DATA AND DISCUSSIONS

A. Semiconductor Material and Device Study

1. General:

During the second quarter of the contract effort was directed toward decreasing contact resistance and increasing the volt-ampere characteristic slope in silicon p-n junction structures. Investigation of the effects of starting material resistivity on forward biased junction characteristics was continued and extended to include lower resistivity silicon and germanium. Cell equalizers and anti-reversal devices were designed and operated with the 3.2 ampere hour nickel cadmium system.

2. Contact Resistance:

Based on static and mercury relay current interruption tests the major contribution to the resistive component of device impedance appears to be that of contact resistance. Ohmic contacts of good quality, electrically and mechanically, are obtained by the electroless nickel plating process. Two layers of nickel are required, the first layer being sintered prior to application of the second plating step. The sintering had previously been done at 900°C. Phosphorus present in this type nickel may at this sintering temperature, tend to diffuse into and compensate the p type silicon at the nickel interface effectively increasing contact resistance. Sintering experiments and the results reported by others[3] indicate 500°C sintering temperature optimum in the case of low resistivity p type silicon. Photomicrographs utilising angle lap technique indicate adequate alloying at this temperature. The effect of sintering temperature is indicated by the following table which compares equalizers made from the same silicon crystal but sintered at 500°C and 900°C. Crystal resistivity was 0.01 ohm-cm and sintering time was 30 minutes in both cases. Run S 30114-2 units were constructed of two lead bonded dice; units of run S 21214-0 were constructed of single dice and data calculated on the basis of single dice measurements.

TABLE I

Measured Data for Two Experimental Equalizers

S 30114-2 #2 - 500° Ni. Sinter			S 21214-0 #1 - 900°C Ni. Sinter		
J amp/in^2	Volts	M(ΔJ=300-100) amp/volt/in^2	J amp/in^2	Volts	M(ΔJ=300-100) amp/volt/in^2
300	1.705	2.67×10^3	300	1.744	1.75×10^3
100	1.630		100	1.630	
30	1.550		30	1.538	

Volt-Density data, obtained over a wider measurement range are shown plotted in Figure 1. Slope of the curve is somewhat greater for the unit sintered at 500°C, particularly at higher current densities. The diode equation, solved for N, gives 1.26 and 1.45 for this junction parameter for 500°C and 900°C sintering temperatures respectively. The mercury relay current interruption test did not provide discernible difference in device resistive components due to relatively low resolution.

Some difficulty in obtaining complete wetting of the electroless nickel was encountered in dice bonding experiments utilizing pure lead as the bonding agent. Consequently, subsequent dice have been plated with approximately 50 micro-inches of gold prior to bonding. Use of the gold plate provides excellent wetting by the lead as well as reducing the amount of lead required.

3. Starting Material Resistivity:

This study was extended to lower resistivities ranging from 0.0004 to 0.01 ohm-cm silicon and 0.0005 to 3 ohm-cm germanium. Results obtained in the case of silicon are best considered by reference to Figure 2 in which typical room temperature test data are plotted for 0.0004, 0.005, and 0.009 ohm-cm p type starting silicon. Process steps were held as nearly identical as possible in all cases. All units were two dice bonded structures mounted in the standard 7/16 inch stud mount package and attached to Delta HC403 heat sinks during testing. No junctions suitable for equalizer application have been obtained or really expected because of the diffusion technique employed, from the 0.0004 ohm-cm silicon. Linearity of the 0.009 ohm-cm device is better than that of the 0.005 ohm-cm counterpart; current rise per voltage increment is greater in the 0.005 ohm-cm device. Saturation current is about 4×10^{-9} amperes in both cases. Slightly lower N values of 1.32, and greater slopes of 5×10^{3} amperes/volt/in^{2} were obtained from the 0.005 ohm-cm devices.

Work on germanium was limited to 0.0005 ohm-cm p type and 2.0-3.0 ohm-cm n type material during this period. As in the case of silicon, devices suitable for the present application have not been obtained from the very low resistivity material. Specific voltages as a function of starting material resistivity have not been demonstrated; virtually the same volt-ampere characteristics have been obtained from 2 ohm-cm and 37 ohm-cm starting germanium. A small pyrex enclosed alloy furnace has been fabricated to allow observation and optimization of the alloy process.

B. <u>Prototype Device Fabrication and Evaluation</u>

1. General:

All equalizers fabricated during this period have been mounted on the standard 7.16 inch diode studs. The lead wire, connecting top of dice and package egress has been redesigned and the resistance reduced to about 4×10^{-4} ohm. Anti-reversal devices have been packaged in the DO1 package. Junction area has been held to 0.024 in^2 in the silicon devices and to 0.005 in^2 in the germanium devices. Junctions in silicon were of the diffused type; those in germanium were alloyed.

2. Testing:

Testing with the following exceptions, has been as previously reported and to avoid repetition reference is made to the foregoing quarterly report.

The reported method of determination of junction saturation current, necessary for evaluation of N of the diode equation, assumed zero surface leakage under conditions of a small reverse bias. In practice, the surface leakage does not equal zero and due to the low order of magnitude of saturation current effectively masks this quantity. A more valid assumption is that over the linear portion of the junction volt-log ampere curve surface leakage current is an insignificant part of the total device current. The linear portion of this curve, extrapolated to the zero volt intercept, gives the thermally generated current through the junction or the saturation current. The diode equation can then be solved for N, at room temperature, by

$$N = \frac{38\,V}{\ln \frac{I}{I_s}}$$

Where N = exponent compensation (diode equation)

V = voltage applied across junction

I = total junction current

I_s = junction saturation current

3. Battery Charging Circuits:

Three battery charging circuits, all utilizing sealed rechargeable nickel cadmium D size cells, have been fabricated and operated. These sintered plate cells are rated by the manufacturer as follows:

Average Capacity to 1.0 Volt	3.2 A.H. at 1 hour rate 4.0 A.H. at 5 hour rate
Recommended Charge	Constant Current 400 MA for 14 hours

Constant current to constant voltage charge methods[1,2] are indicated to safely store maximum energy in minimum time. The average ampere hour reinsertion for the nickel cadmium system has been established as 130% the removed ampere hours; the limiting charge voltage at room temperature has been determined to be 1.48-1.52 volts.[1,2]

The 90 minute cycle, 55 minute charge - 35 minute discharge, was used in all tests. Discharge depth was 75% rated capacity. On the basis of the 90 minute cycle and 130% reinsertion the charge and discharge currents were calculated as

$$I_c = \frac{3.2 \text{ amp. hr. x } .75 \text{ x } 1.3}{\frac{55}{60}\text{ hr}} = 3.4 \text{ amperes}$$

$$I_d = \frac{3.2 \text{ amp. hr. x } .75}{\frac{35}{60}\text{ hr}} = 4.12 \text{ amperes}$$

The one hour rate, while possibly unfair to the cells, was used in calculating the charge and discharge currents in the interest of obtaining the most data in the shortest time.

As a preliminary test two randomly selected cells without the protective devices were connected in series and cycled several times under constant voltage to constant current conditions. Typical measured data are plotted in Figure 3.

The first battery and control circuit constructed, designated BCC-1, employed three cells in series with equalizers and anti-reversal devices across each cell. The semiconductors were mounted in a ribbed heat sink, having 44 in^2 surface area, not thermally connected to the cells. Discharge was into a constant load which was adjusted to give an average 4.12 ampere discharge current. This circuit was operated over several cycles and while cell terminal voltage was clamped to the specified level, inadequacy of the heat sink arrangement was apparent. The great difference in cell and equalizer thermal capacities require, that to track thermally, the cases of these devices be connected through a path of low thermal resistance. Ampere hour accounting becomes quite involved when constant load discharge is employed; these preliminary tests also indicated the need of constant current discharge at least during the initial stages of the investigation.

In circuit BCC-2 subsequently built and tested, the semiconductor devices are bolted to 0.25" x 1.5" x 2.125" copper plates having drilled holes to accomodate the nickel cadmium cells. The plates are clamped to the cells by means of an integral slot and set screw. Thermal gradients between cells and associated equalizers are minimized. Figure 4 shows the experimental circuit.

Five of the 3.2 ampere hour nickel cadmium cells are connected in series in the circuit; equalizers and anti-reversal devices are connected across three cells only. Table II is a location chart of the circuit components.

TABLE II

Location Chart BCC-2 Components

Cell	Position	Equalizer	Anti-Reversal
9	1	S 30121 #1	AR30207 #2
7	2	S 30121 #2	AR30207 #4
5	3	S 30121 #6	AR30207 #7
8	4	None	None
6	5	None	None

The circuit has been cycled at 30, 80, and 120 degrees Fahrenheit under the following conditions: Ninety minute cycle; 130% ampere-hour (to circuit) reinsertion; 75% discharge depth; and constant current discharge. Terminal voltages, cell temperatures, and current distributions were read and recorded at five minute intervals. Third cycle test data which are typical are plotted in Figures 5 through 8. Figures 5 and 6 show individual terminal voltages as time functions for protected and unprotected cells respectively; Figures 7 and 8 show instantaneous cell case temperatures over the cycle for protected and unprotected cells respectively. Instantaneous equalizer currents during charge are plotted on Figure 5. Cell 7 has shown a tendency to reverse near the end of discharge both with and without its equalizer connected. The enamel finish was dried in an oven which inadvertently reach 150°F; it is not known whether or not this damaged the cell. Reverse voltage of this cell was clamped to less than 0.4 volts in all cases of complete reversal. Referring again to Figures 7 and 8, the average protected cell temperatures were: #9, 98°F; #7, 101°F; and #5, 98.5°F. The average unprotected cell temperatures were: #8, 100°F; and #6, 99°F. Tested at 30°F, the maximum cell voltage obtained with equalizer was 1.60 volts; the maximum without was 1.70 volts. At 120°F ambient, maximum terminal voltages of 1.45 and 1.49 with and without equalizers respectively were reached.

Six series connected groups of two paralleled 3.2 ampere hour nickel cadmium cells are utilized in the third battery and control circuit designated BCC-3. While it is recognized that generally parallel operation of the sealed batteries is unsatisfactory, this test is expected to provide information as to feasibility of operating the semiconductors in parallel and information with respect to the effect of the semiconductors on paralleled cells. Only six 90 minute cycles at 75% discharge depth have been completed. Charge current has been set to 6.8 amperes; discharge current is 8.24 amperes. Figure 9 is a photograph of the battery and control circuit.

A brief summary of the third cycle data is shown below. Equalizers and anti-reversal devices are connected across groups 1, 2, and 3 but not across groups 4, 5, and 6.

TABLE III

BCC-3 Third Cycle Data

Group		1	2	3	4	5	6
End of Charge							
	Voltage	1.50	1.49	1.50	1.54	1.54	1.51
	Equalizer Amperes	2.19	1.60	1.79	--	--	--
	Temperature (F)	105	105	103	106	112	105
End of Discharge							
	Voltage	1.15	1.02*	1.16	1.05	1.16	1.05*
	Temperature (F)	99	103	100	108	105	106

*Reversed before measurements were completed.

III. PROGRAM FOR NEXT INTERVAL

1. The study of semiconductor material and junction structures applicable to present effort will be continued with emphasis on the lower resistivity starting material.

2. Higher voltage devices suitable for use with the silver-zinc couple will be designed.

3. Additional experimental structures will be fabricated and evaluated.

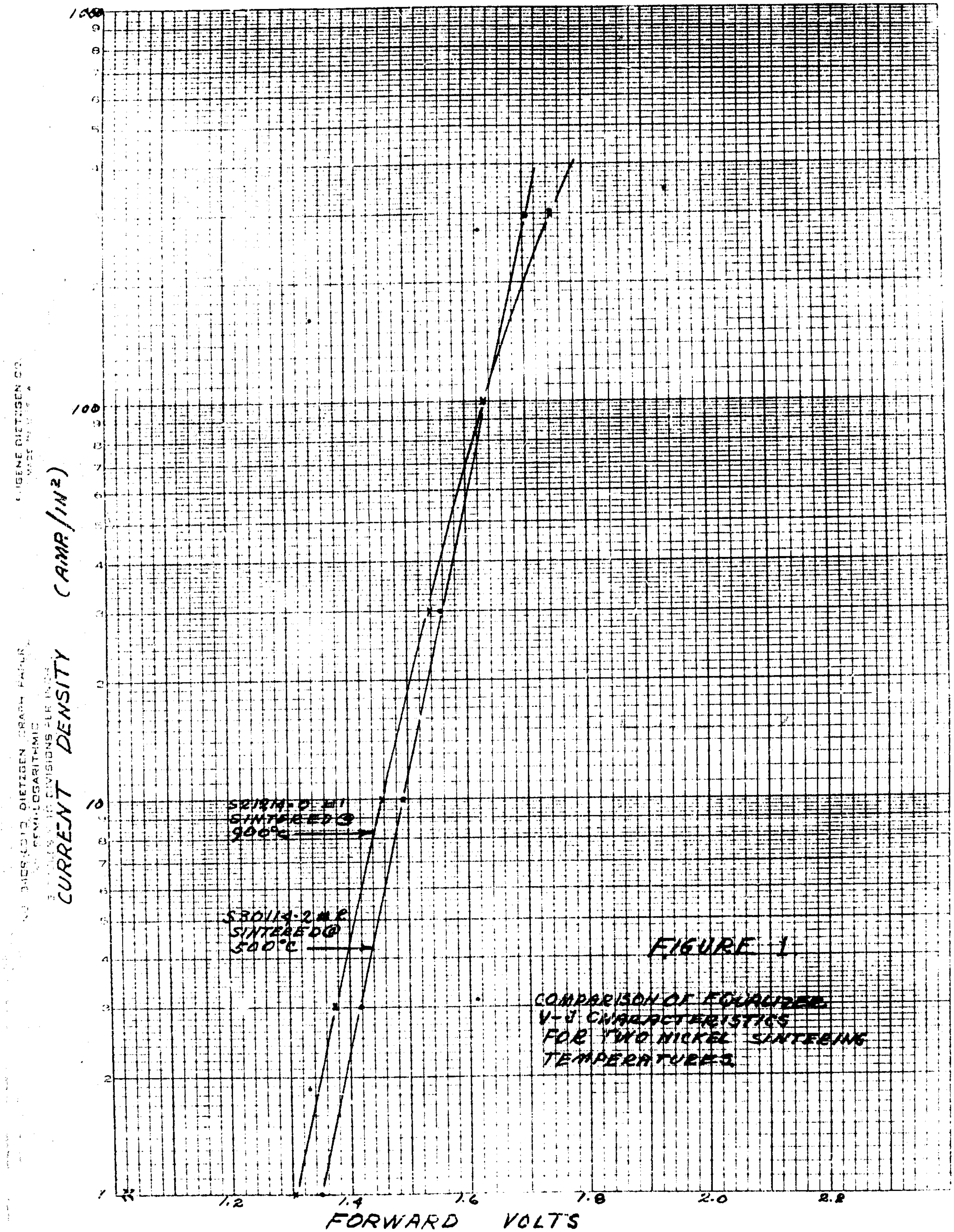

FIGURE 1

COMPARISON OF EQUALIZED V-J CHARACTERISTICS FOR TWO NICKEL SINTERING TEMPERATURES

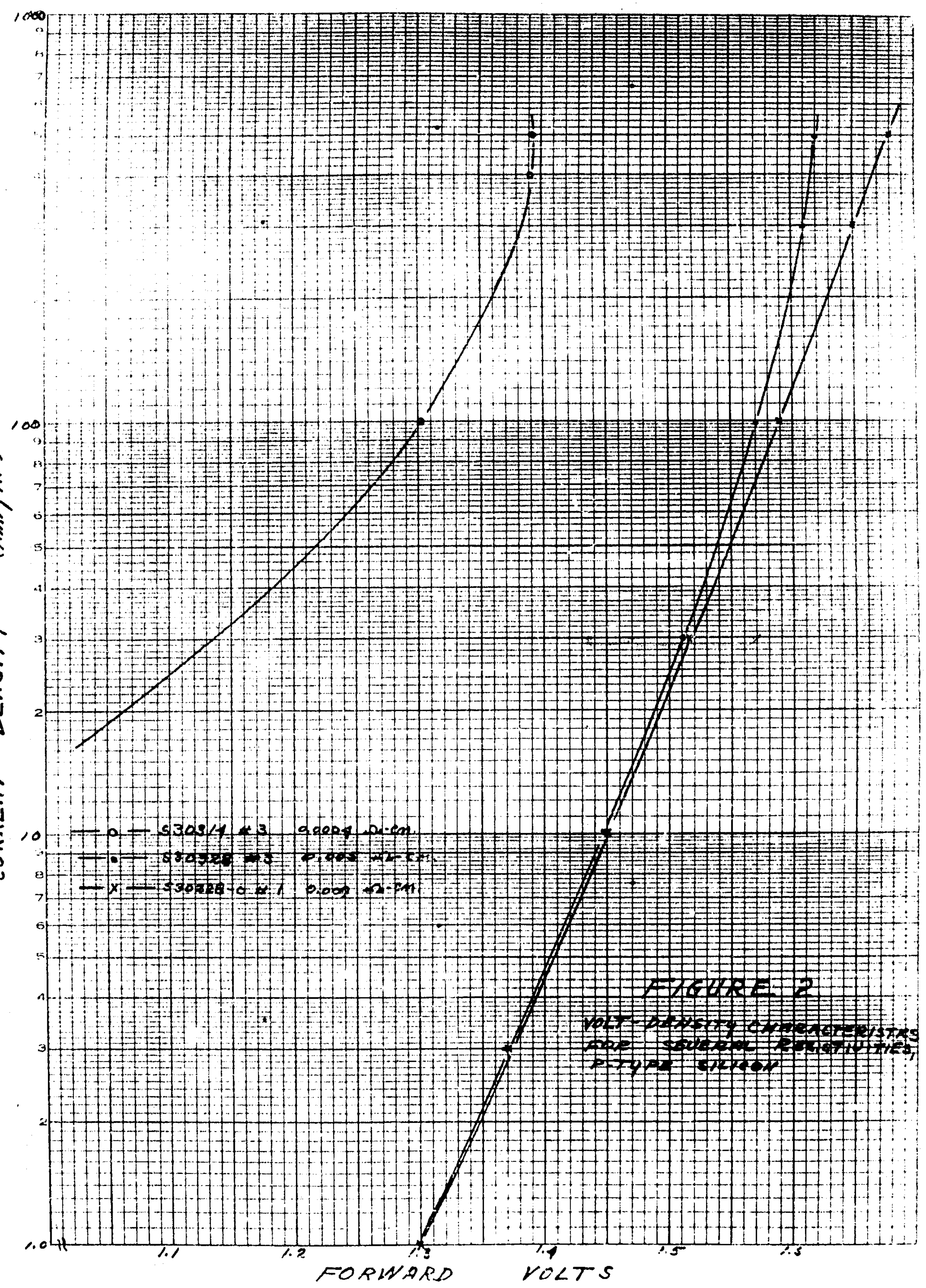

FIGURE 2
VOLT-DENSITY CHARACTERISTICS FOR SEVERAL RESISTIVITIES, P-TYPE SILICON

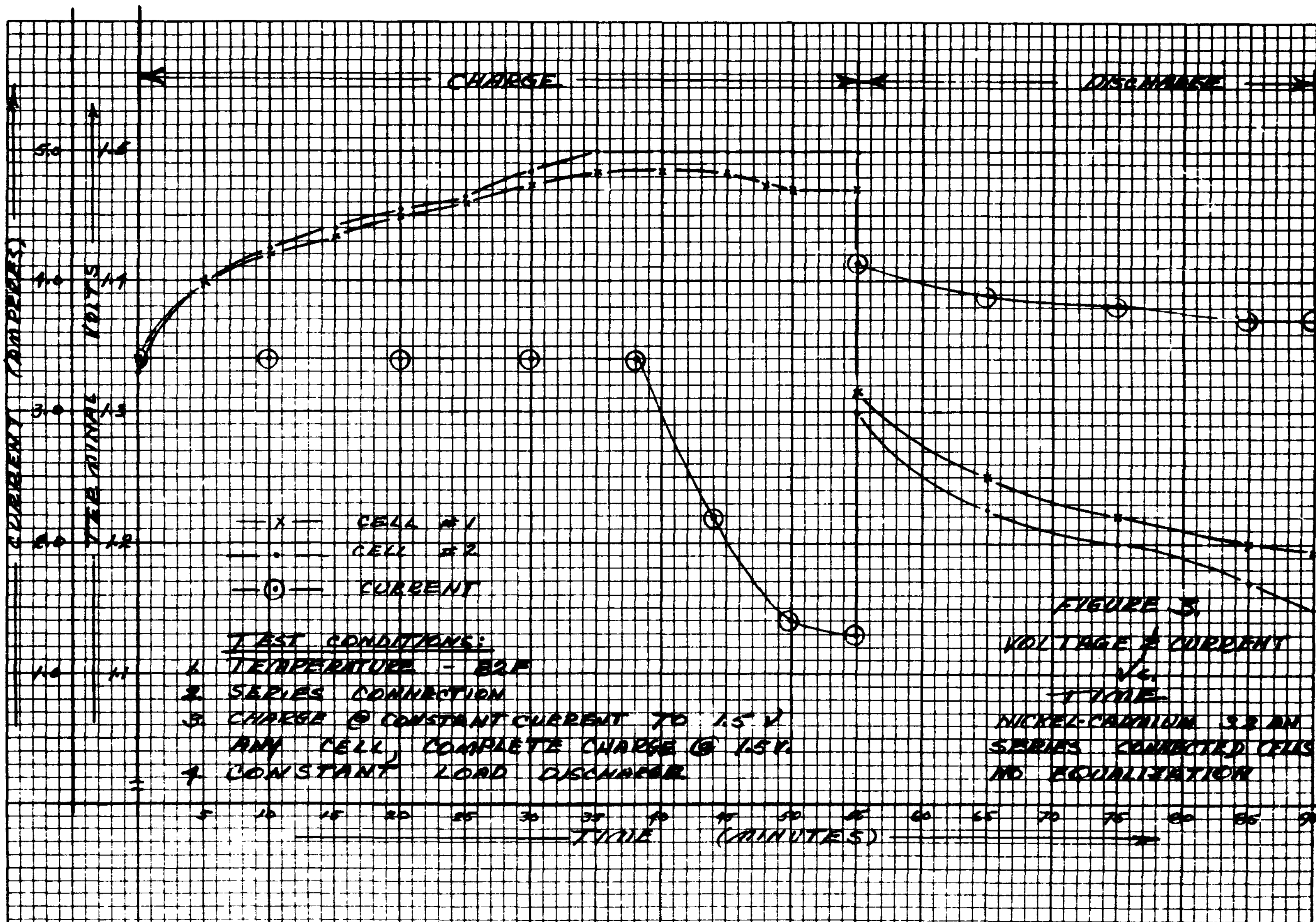
CHARGE
DISCHARGE
CURRENT (AMPERES)
TERMINAL VOLTS
5.0
4.0
3.0
2.0
1.0
1.5
1.4
1.3
1.2
1.1
CELL #1
CELL #2
CURRENT
TEST CONDITIONS:
1. TEMPERATURE - 82F
2. SERIES CONNECTION
3. CHARGE @ CONSTANT CURRENT TO 1.5 V
ANY CELL, COMPLETE CHARGE @ 1.5V.
4. CONSTANT LOAD DISCHARGE
FIGURE 5
VOLTAGE & CURRENT
Vs.
TIME
NICKEL-CADMIUM 3.3 AH
SERIES CONNECTED CELLS
NO EQUALIZATION
5
10
15
20
25
30
35
40
45
50
55
60
65
70
75
80
85
90
TIME (MINUTES)

Figure 4

Battery and Control Circuit BCC-2

Equalizers and anti-reversal devices are mounted near the top of copper plates. Cell cases were treaded as follows: Position 1 (right): Nickel plated as recieved; 2: Copper flash, 1 mil silver plate, black enamel; 3, 4, and 5: Copper flash, 1 mil silver plate. Thermo couples are attached to each cell near the copper mounting plate

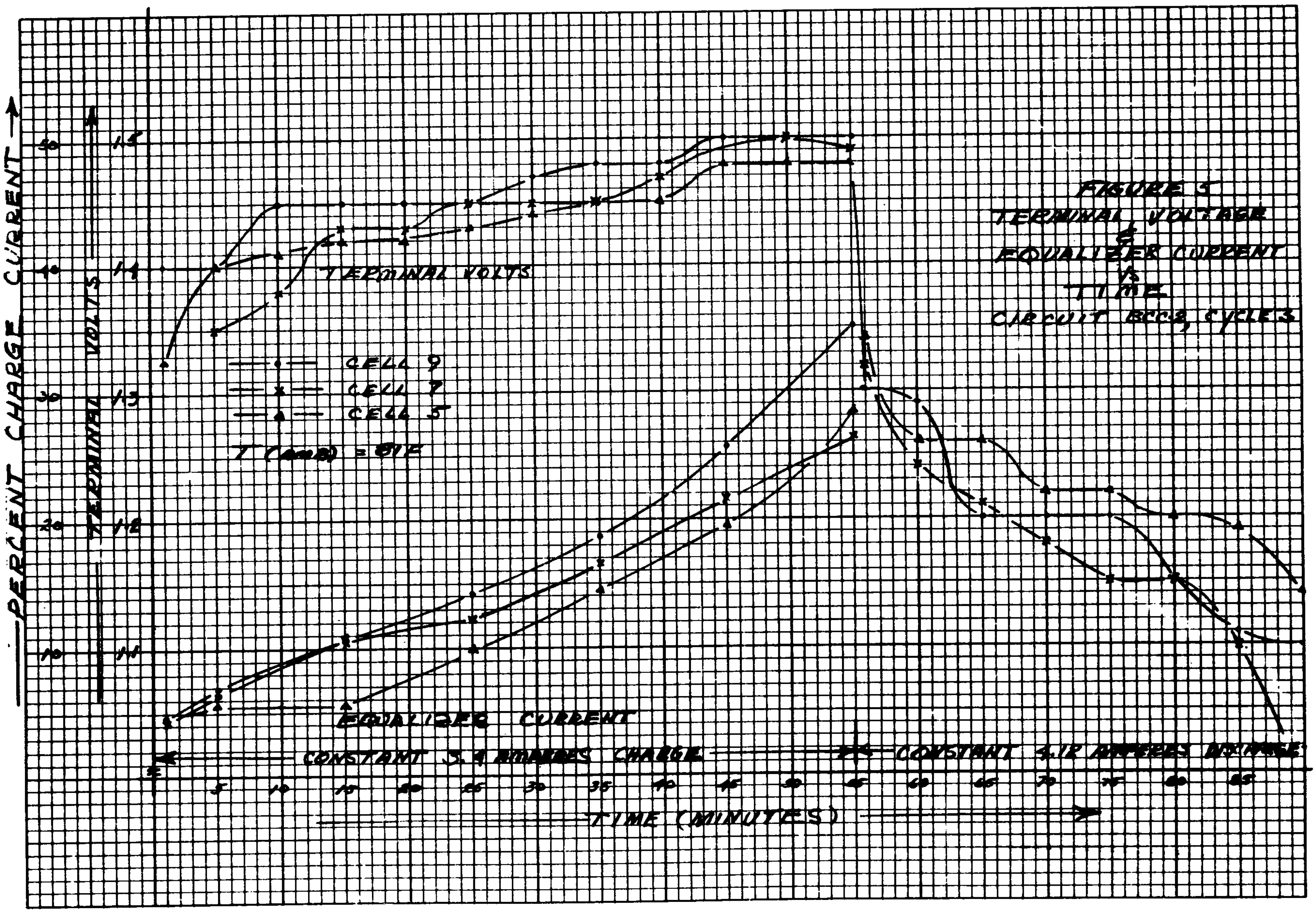
FIGURE 5
TERMINAL VOLTAGE
&
EQUALIZER CURRENT
VS
TIME
CIRCUIT BCC2, CYCLE 3
TERMINAL VOLTS
CELL 9
CELL 7
CELL 5
EQUALIZER CURRENT
CONSTANT 3.4 AMPERES CHARGE
CONSTANT 4.12 AMPERES DISCHARGE
TIME (MINUTES)
PERCENT CHARGE CURRENT
TERMINAL VOLTS
1.5
1.4
1.3
1.2
1.1
50
40
30
20
10
5
10
15
20
25
30
35
40
45
50
55
60
65
70
75
80
85

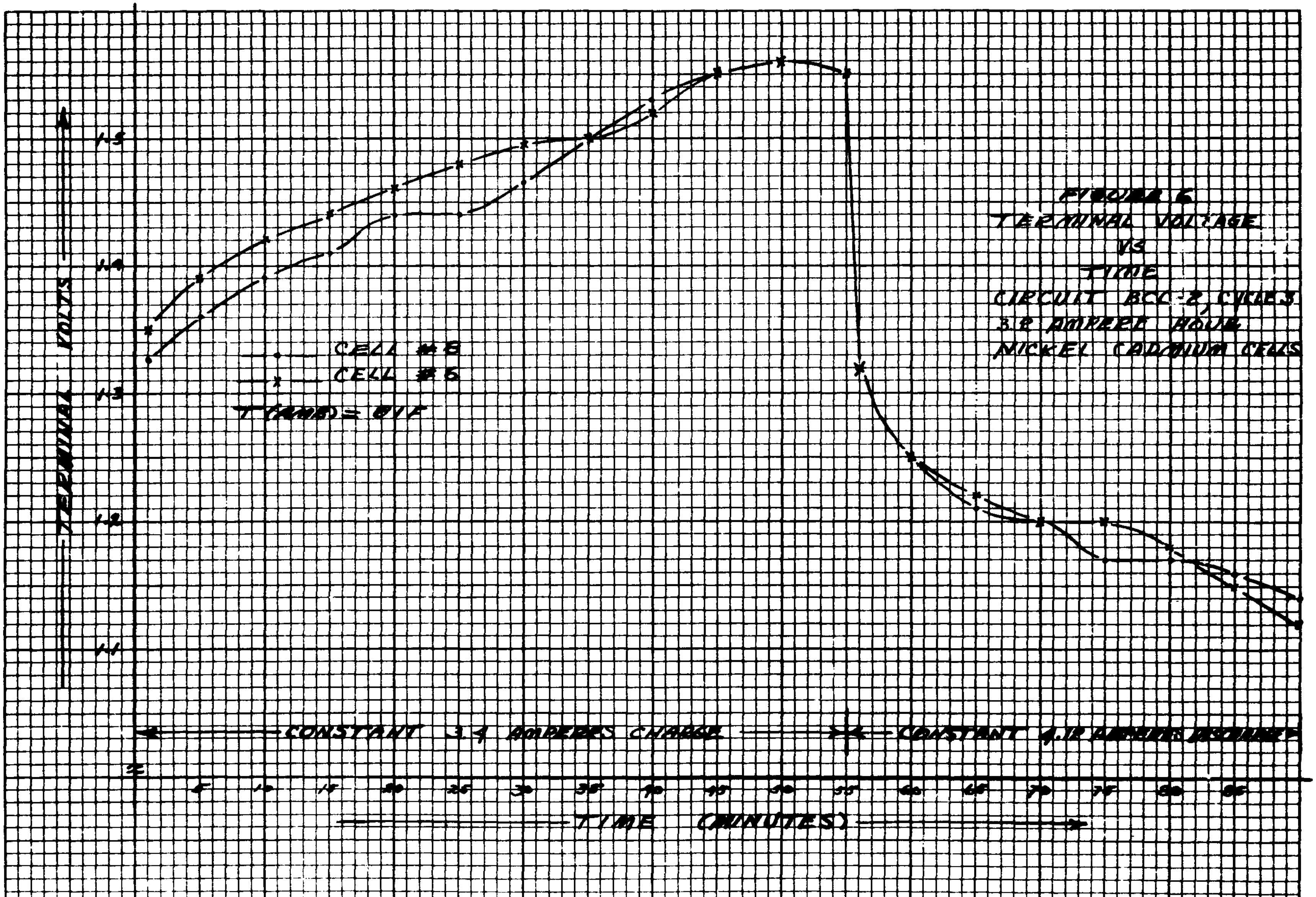
FIGURE 6
TERMINAL VOLTAGE
VS
TIME
CIRCUIT BCC-2, CYCLE 3
3.2 AMPERE HOUR
NICKEL CADMIUM CELLS
CELL #8
CELL #6
TERMINAL VOLTS
1.5
1.4
1.3
1.2
1.1
CONSTANT 3.4 AMPERES CHARGE
CONSTANT 4.12 AMPERES DISCHARGE
5
10
15
20
25
30
35
40
45
50
55
60
65
70
75
80
85
TIME (MINUTES)

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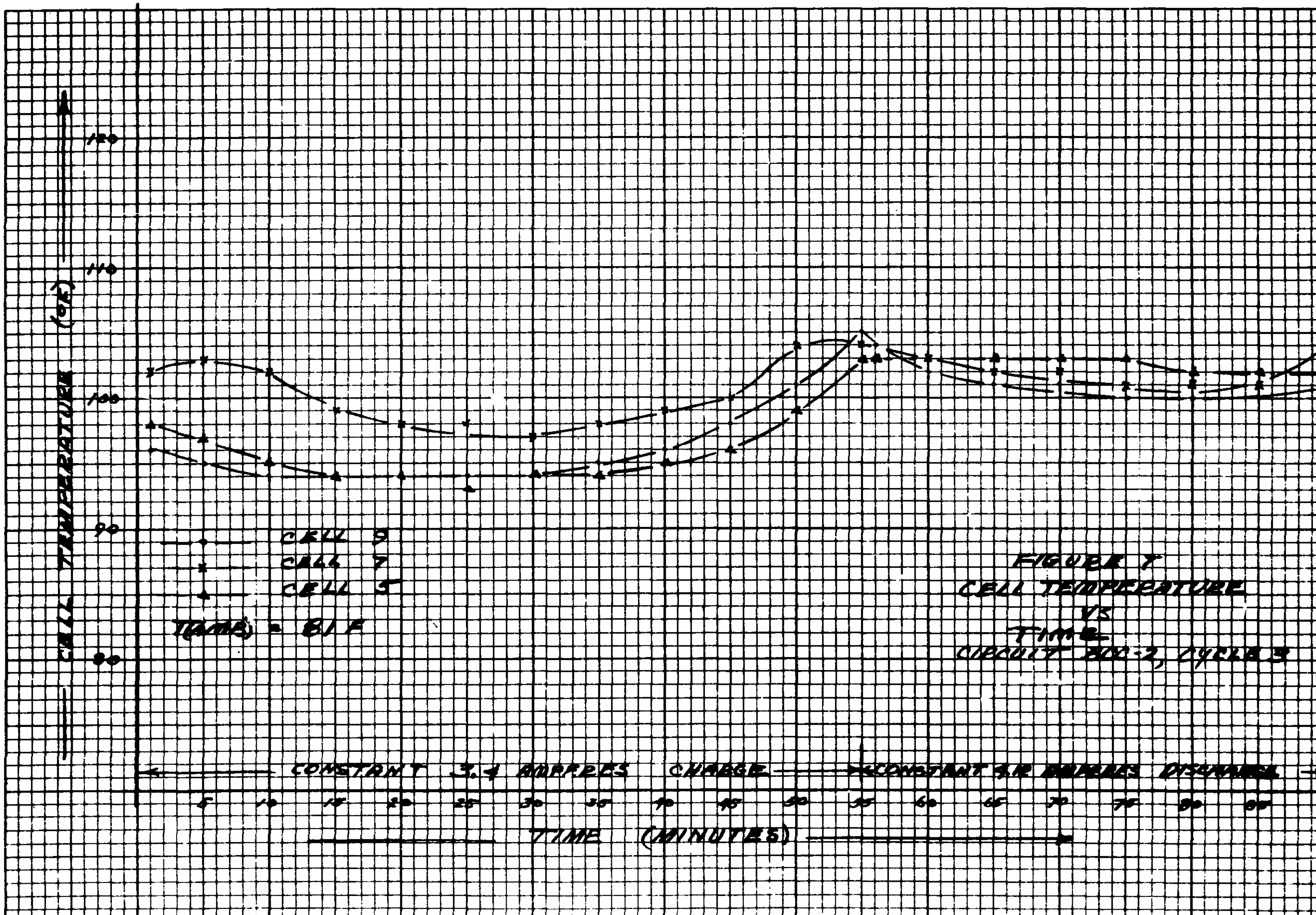

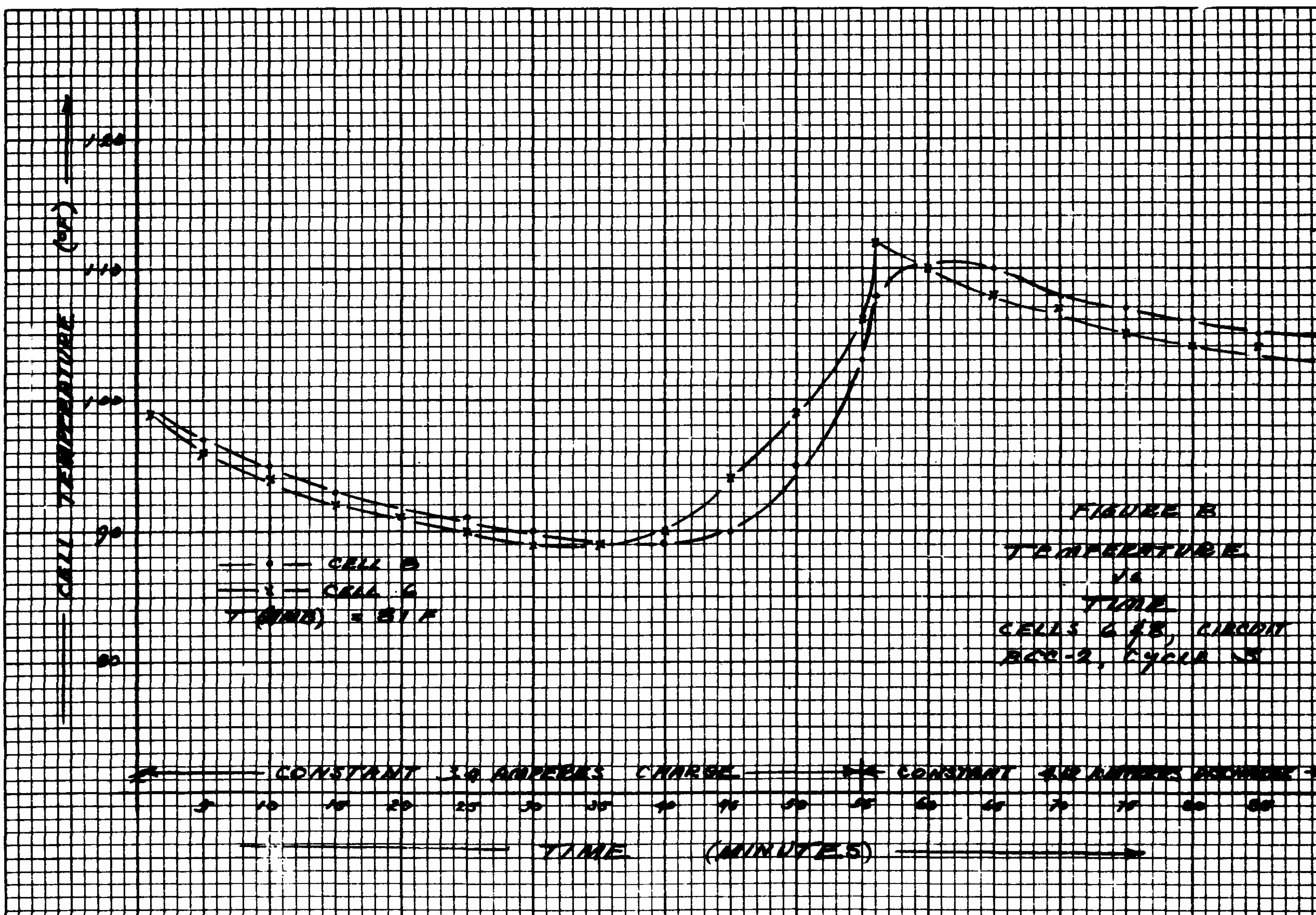
FIGURE B
TEMPERATURE
vs
TIME
CELLS 6 & B, CIRCUIT
BCC-2, CYCLE 3
CELL B
CELL 6
CELL TEMPERATURE (°F)
80
90
100
110
120
CONSTANT 3.0 AMPERES CHARGE
CONSTANT
5
10
15
20
25
30
35
40
45
50
55
60
65
70
75
80
85
TIME (MINUTES)

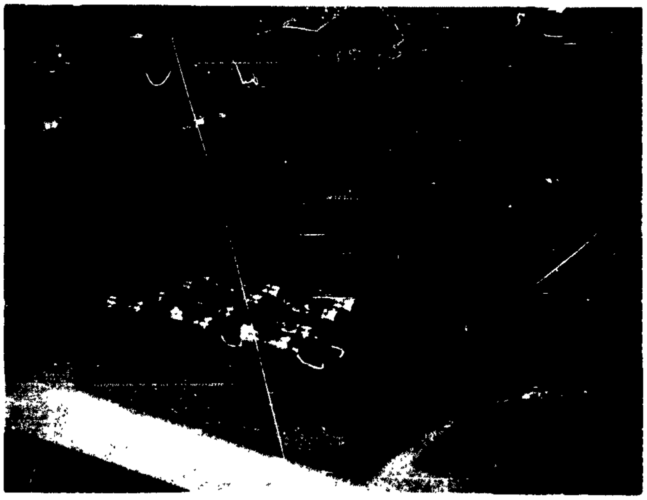

Figure 9

Battery and Control Circuit BCC-3

Cells and semiconductors are mounted in six copper plates 2 25" x 3" x 0.25", each parallel set being mounted in a separate plate.

REFERENCES:

1. W. W. Clark, W. G. Ingling, I. F. Luke, R. Leaf, "Alkaline Battery Evaluation", ASD-TDR-62-893, October 1962.

2. I. F. Luke, Inland Testing Laboratories, Dayton, Ohio, letter dated 4 December 1962.

3. M. V. Sullivan and J. H. Eigler, "Electroless Nickel Plating for Making Ohmic Contacts to Silicon", J. Electrochemical Society, Vol. 104 #4, pp. 226-29, April 1957.

4. J. M. Booe, W. D. Loftus, "Cell Equalization Techniques", Contract No. AF 33(657)-8749 Quarterly Technical Progress Report No. 1.

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